A Configurable Test Bed Platform for Test and Validation of Payloads for Nanosatellites

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***Abstract*— This work proposes a design and implementation of a configurable test bed composed of communication protocols, memories and connections synthesized into a commercial flash-based FPGA for use in space applications. The intention of this platform using modular blocks is to decrease the development time and increase the flexibility and reprogrammability, when compared to ASICs circuits. The system is been designed to comply with NanoSatC-BR1 nanosatellite mission, the first Brazilian Cubesat. The FPGA will control the entire payload board. Previous in loco tests demonstrated the functionality of this configurable test bed applied to Cubesat application.**

***Index Terms*— Nanosatellite, Cubesat, NanoSatC-BR1, FPGA, COTS.**

I. INTRODUCTION

The use of small satellites has increased substantially in the past years due to the reduced cost in development and launch and the flexibility offered by commercial components. Futhermore, the standardization of Cubesat systems and the development of easier integrated devices, such as the Space Plug-and-play Architecture (SPA) set of circuits, is decreasing significantly the time-consuming component of spacecraft development [1]. The use of FPGAs in different phases of nanosatellite projects corroborate to save time and costs, due to the flexibility and reprogramabillity, either for test and validation phases or for the flight model of the satellite. In addition, the modern high performance FPGAs can implement a complete system for spacecraft onboard computation. A System-On-Chip (SOC), composed of hard microprocessors, high density embedded memories, analog and digital components can be described in the programmable architecture of the FPGA, benefiting the subsystems integration and reducing the design complexity. Other benefit is that FPGAs are a less expensive option than traditionally utilized devices such as Application Specific Integrated Circuits (ASICs) [2].

This work came from the need to reduce the complexity of validate new custom cores and ease the integration and control new commercial devices in the payload board. To this end is proposed a configurable test bed platform, based in a flexible FPGA architecture.

It is well-known that FPGAs working in spatial environment are affected by long term ionizing damage and transient ionization, due to their interaction with the spectrum of radioactive particles [3][4]. But the protected options of devices for space application are multiple times more expensive than Commercial Off The Shelf (COTS) components, sometimes they are unavailable for purchase and surely unviable economically for nanosatellite projects. Considering the radiation dose that satellites operating at Low Earth Orbit (LEO) are facing [5][6], in many cases it is possible to use circuits COTS with some radiation hardening technique, which were robustness prequalified.

This work designed and implemented a configurable test bed platform, aimed for a commercial Flash-based ProASIC3E FPGA Family from Microsemi. This FPGA family is not space-flight qualified, but tests have been made under Total Ionizing Dose (TID) showing it robustness up to 25 krads(Si) [7]. When considering neutron and alpha particle hitting, Flash-based FPGAs provide immunity to configuration loss due to Single Event Effects (SEE) [8].

The test bed platform allows components to be evaluated and tested in space. As a flexible system, it can be adjusted a wide array of and quantity of components and interfaces, suitable for test and evaluation of different commercial circuits within nanosatellites. The development of such platform allows developers to reduce the efforts in the integration of

components and therefore speed up the overall system development time.

This adaptive system ease the control of new payloads and softcores for test and validation in space, and the integration can be readily performed, through configuration parameters. It is intended for modularity. Each component connected to the test bed can have a specific interface programmed using a hardware description language (HDL). The data of each component is stored in embedded memories and each component has its own memory space reserved. The size of the allocated memory can be also configured. The data transfer priority can be set and packaging can also be added to the logic, when needed. Communication with peripheral devices and the onboard computer is done through the pre-implemented protocols, such as I2C, SPI and external memory control.

In the first application of the test bed two components are connected to the controller FPGA: a commercial magnetometer and a hardened test chip. The FPGA has embedded a microprocessor and a few other soft cores to be used in space. This test bed will be used in the NanoSatC-BR1, the first Brazilian Cubesat scheduled to be launched in mid-2013.

II. THE DEVELOPED CONFIGURABLE TEST BED DESIGN

The ProASIC3E from Microsemi is a Flash-based family of FPGAs which offer low-power and low-cost COTS solution. Based on nonvolatile technology, the ProASIC3E is far less susceptible to radiation induced failures than Static Random Access Memories (SRAM) based FPGAs. Besides, the Flash-based devices retain their configuration when power is removed from the FPGA, whilst the SRAM-based lose their data and configuration and need to be reprogrammed during power-up. Despite the configuration retaining of the ProASIC3E FPGA, it has some blocks of radiation unhardened embedded SRAM available for user applications.

Microsemi Corporation provide some IP Cores within their Libero IDE development tool which implements different features, like bus interface controllers, clock management, digital signal processors (DSP), memory controllers, error detection and correction (EDAC) blocks, peripheral communication protocols, soft processors, etc.

Some of Microsemi IP Cores were implemented for the control, management and communication with different commonly used nanosatellite payloads. Customized cores can be incorporated to the FPGA to test and validate new payloads before flight. Applying these Microsemi IP Cores and the implemented configurable blocks, the modularity is achieved, since the functionality configuration of each module is done through parameters, and can be altered to comply with new project objectives.

There are several modules performing different tasks, so, the property of specify the memory space to each module was designed. Each module can have its own dedicated memory embedded, and its size is configurable (within the range of available SRAM) from module to module, and the reading and writing of data can be done either by the module or by a central

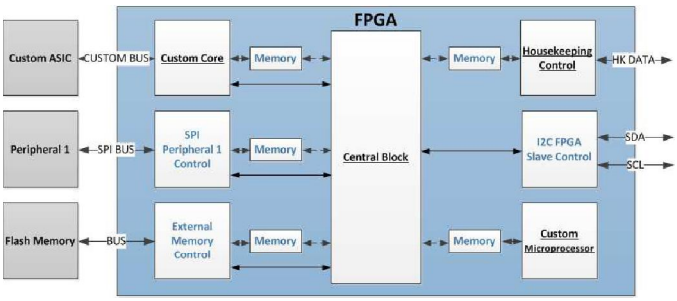

Fig. 1: Configurable test bed platform designed.

block control. Also, memory spaces division improves the reliability of the system, once that a transient fault in one module's memory should not affect the others modules.

The central block controls and communicates with the remaining modules present in the FPGA, and the changing of functionalities or addition of new payloads to the project is by altering these configured parameters in the top module of the design and in the central block, and occasionally adding some features into the specific modules.

Figure 1 exemplifies some functional blocks implemented within the FPGA.

III. THE NANOSATC-BR1 MISSION AND THE PAYLOAD DEVELOPMENT DESCRIPTION

The NANOSATC-BR is the first Brazilian Scientific Nanosatellite. The concept was developed to monitor, in real time, the Geospace, the particle precipitation and the disturbances at the Earth's magnetosphere over the Brazilian Territory, and the determination of their effects on regions such as the South Atlantic Magnetic Anomaly (SAMA) and the Brazilian sector of the Ionosphere Equatorial Electrojet [9].

In order to monitor the SAMA disturbances, the satellite's first payload will consist of a magnetometer, the XEN1210 from Xensor Integration. The magnetometer control interface is fully digital, and the readout and programming are performed via SPI protocol.

The second payload will consist of a Brazilian radiation-hardened test chip, entirely designed by Santa Maria Design House (SMDH). It is intended to both validate the in-flight functional correctness and check the sensibility of this specific circuit to TID and SEEs. After the validation of this circuit, it will be rather used on others Brazilian satellites.

Finally, the last payload to be mentioned is the ProASIC3E, the FPGA from Microsemi. The FPGA will centralize the control of other payloads, configuring the test bed design for such end. Figure 2 depicts the payload board functional blocks.

The payload board contains some others circuits: sensors for housekeeping, electrical connection regulators, analog to digital converters and clock source.

Besides the previously cited payloads and circuits present in the board, the FPGA will also embed a fault-tolerant MIPS softcore for in-flight validation. This custom softcore is 32-bit microprocessor adapted version of the well-known MIPS architecture, with a non-intrusive hybrid fault detection approach that combines hardware and software techniques to detect transient faults in the microprocessor. Fault injection

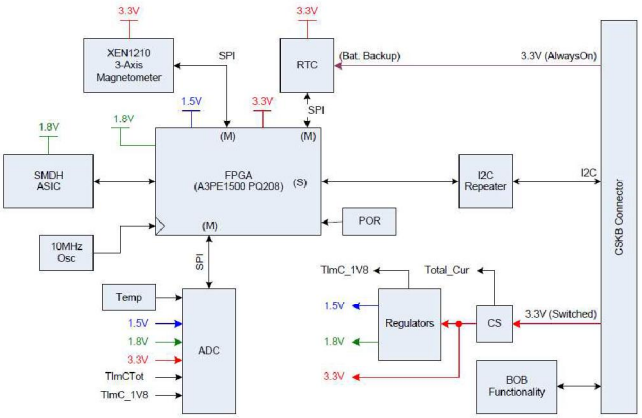

Fig. 2: Payload board functional blocks. Logical connection between circuits and voltage supply is presented.

tests shows the efficiency of this method on detecting 100% of faults, and minimal memory area and execution time overhead compared to original MIPS architecture [10].

The detailed modules of the FPGA are demonstrated in Fig. 3.

IV. CURRENT DEVELOPMENT STATUS OF NANOSATC-BR1

The case study payload test bed for NanoSatC-BR1 was partially developed and synthesized for the part A3PE1500-PQ208, and included the controllers for magnetometer, SMDH ASIC, MIPS and I2C slave interface. It resulted in the occupation of 21,281 Versatiles (55% available in this part, which implement approximately 831,269 equivalent logic gates), 51 user Inputs/Outputs (34.7% of available IOs), 1 PLL (out of 2) and 39 blocks of embedded SRAM (from a total of 60 4,608-bit blocks).

A clock source of 10MHz for the payload is supplied and is compliant with the NanoSatC-BR1 requisites. Nevertheless, a maximum frequency of more than 20MHz is achievable for the entire payload system, but this higher frequency is not necessary and not desired for the sake of energy reserve.

The complete placement and floorplanning is illustrated in the Fig. 4.

The post-place and route simulation was performed through

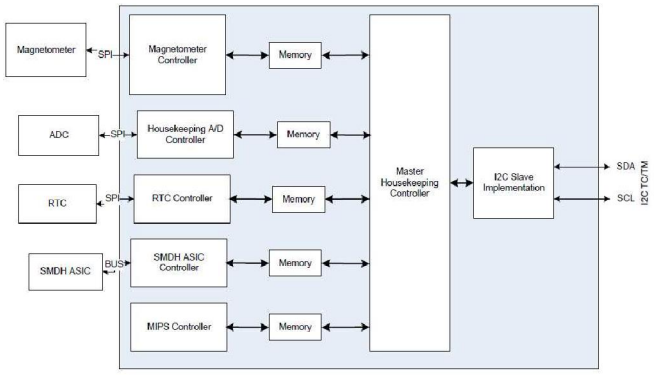

Fig. 3: FPGA functional blocks. Within the FPGA is detailed the cores interfacing with external peripherals (payloads and housekeeping sensors).

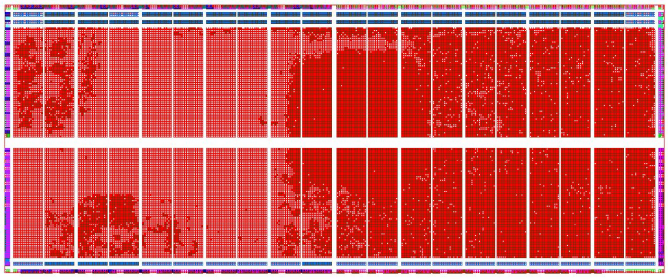

Fig. 4: Complete placement of the designed test bed FPGA.

Modelsim, with a simulation model emulating a OBC requisition and I2C data transmissions, magnetometer readouts, MIPS computations and SMDH ASIC transactions, all in parallel. The generated vsim file was used as input into SmartPower tool, to calculate the power consumed for the device. The result is 152mW of total power consumption with the temperature of 70 degrees Celsius.

CONCLUSION AND FUTURE WORK

A proper system operation could be demonstrated. Several functional tests was performed connecting the test bed platform to the magnetometer payload, and interfacing ProASIC3E test bed to other FPGA through I2C bus. The second FPGA simulated the NanoSatC-BR1 onboard computer (OBC). The SMDH ASIC behavior was emulated inside the ProASIC3E (since the test chip was not available during the test setup). The FPGA OBC requested data from FPGA slave (test bed platform) through I2C bus, the same way the NanoSatC-BR1 OBC will request when completed its development. After the request acknowledgment, the ProASIC3E starts to send data from MIPS processing, SMDH ASIC tests and magnetometer measurements, following a prescribed priority.

The data are received in the FPGA OBC and sent back to a computer, and logged to posterior analysis (Fig. 5). The results from MIPS and SMDH ASIC conformed to the golden model, whilst the readouts from magnetometer are compared to other measured sensors in the same environment and were equivalent during all test conditions.

As near future work, the missing modules will be implemented to control the housekeeping circuits. New functional tests need to be performed with the real OBC and the SMDH test chip, and new consumption analysis needs to be remade, considering even orbital patterns and battery capacities.

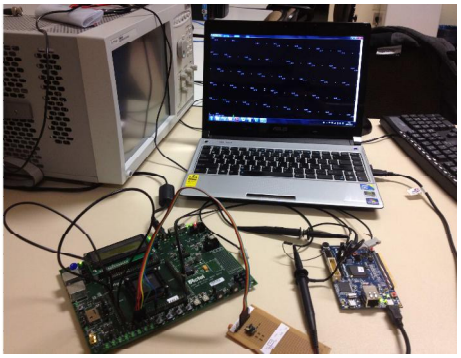

Fig. 5:The experimental setup hardware.

A more generic central block is intended to ease the integration, configuration and control of new payloads and soft cores. The creation of different power modes can optimize the batteries capabilities and/or increase performance.

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